UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/518,642	03/15/2005	Mitsuhiro Yuasa	101249.55749US	2849

23911 7590 03/04/2008

CROWELL & MORING LLP
INTELLECTUAL PROPERTY GROUP
P.O. BOX 14300
WASHINGTON, DC 20044-4300

EXAMINER	
DURBIN, MICHAEL H	
ART UNIT	PAPER NUMBER
2815	

MAIL DATE	DELIVERY MODE
03/04/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/518,642	YUASA, MITSUHIRO	
	Examiner	Art Unit	
	MICHAEL DURBIN	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 November 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) *3,12-15 and 17-23* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1, 2, 4-11 and 16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. **Claims 1 and 16 are objected to because of the following informalities**:

For claim 1, the limitation "pluralities of various types of elements for each type" is unclear and should be reworded. The Examiner suggests: "various types of elements including a plurality of elements of each type" (or something similar).

Appropriate corrections are required.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. **Claim 1 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention**.

4. **For claim 1**, the specification does not adequately describe and support the new matter added to the claim wherein "some of said elements are produced on a substrate by utilizing Micro Electro-Mechanical System technology." Specifically, the specification does not include any support for the elements as referred to in the claim to be made by

a Micro Electro-Mechanical System technology. Applicant points to page 2, lines 1 – 22 and also to page 8, line 25 through page 10, line 10 of the instant specification, but no mention of any Micro Electro-Mechanical System technology or how this may relate to the elements of the claimed invention can be found. Further, the closest to support the Examiner was able to find was from page 6, lines 24 - 29, where the MEMS array is considered to comprise an LCR circuit (the elements). However, this does not support the claimed limitation of formed "by utilizing Micro Electro-Mechanical System technology."

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. **Claims 1 and 2 are rejected under 35 U.S.C. 102(b) as being anticipated by Wallace et al. (US Patent 6,271,728) (hereinafter Wallace)**.

7. **Regarding claims 1 and 2**, figure 11 of Wallace discloses a device array comprising: pluralities of various types of elements (elements such as capacitors and resistors provided in low- and high- pass filters; col. 8, lines 13 – col. 10, line 7) for each type and switches (semiconductor transistors T1, T2, T3, etc. as seen in fig. 11; col. 8, line 55- col. 10, line 7) wherein some of said elements are interconnected by

determining an on/off state of all of said switches so as to make a circuit (fig. 11 shows a phase shifter circuit composed of four stages, and the biasing of the access transistors, or switches, determines how an input signal will be finally filtered based on what the final circuit connected by the open and closed switches comprises).

8. The limitation wherein "some of said elements are produced on a substrate by utilizing Micro Electro-Mechanical System technology," is considered to be a product-by-process limitation. Even though product-by-process claims are limited by and defined by the process, determination of patentability is based on the product itself. The patentability of a product does not depend on its method of production. If the product in the product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product was made by a different process." In re Thorpe, 777 F.2d 695, 698, 227 USPQ 964, 966 (Fed. Cir. 1985), MPEP 2113.

9. In this case, the device of Wallace is capable of having elements (resistors, capacitors, etc.) fabricated by a Micro-Electro-Mechanical System process. Further, Wallace discloses the claimed structure of the invention, thus he anticipates **claims 1 and 2**.

10. **Claims 4 – 11 and 16 are rejected under 35 U.S.C. 102(b) as anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over Wallace, in view of Lucas et al. (US 6,287,951 B1)**.

11. **Regarding claim 4**, Wallace discloses that the device is a fully integrated chipset (col. 3, lines 39-55). It follows that the device will have a semiconductor substrate for the formation of transistors and a conductive interconnect layer to interconnect devices. These limitations are inherent to all integrated semiconductor devices. If Applicant can show that this limitation is not inherent to every integrated semiconductor device, then it would at least been obvious to have a semiconductor substrate and a conductive interconnect layer in order to form a fully integrated device using know techniques. Lucas teaches the use of a device comprising an integrated circuit comprising transistors formed in the substrate (also in the first interconnect level as seen in figure) along with a plurality of elements formed in an interconnect layer (the interconnects are at least resistors). It would have been obvious to modify Wallace with the teachings of Lucas to create a fully integrated device leading to reduced manufacturing costs and reduced size.

12. **Further for claims 4 and 8**, Wallace does not explicitly state that the circuit as seen in fig. 11 has the elements formed in an interconnect layer. It would have been obvious, if not inherent to form the elements in an interconnect layer for the purpose of integrating the device. Also, because the gate stacks of the switches reside in the interconnect level with level contacts the switches, the switches themselves are considered to be provided in the interconnect layer due to this proximity.

13. **Regarding claim 5 and 9**, Wallace discloses that all necessary parts are integrated into the chipset (col. 3, lines 39-55) and that the drive parts are to be provided (col. 8, lines 9-12).

14. **Regarding claim 6 and 10**, Wallace discloses that the device is capable of filtering an input wave (col. 8, lines 13-24).

15. **Regarding claim 7 and 11**, all semiconductor circuits have three-dimensional structures, as they exist in three-dimensions.

16. **Regarding claim 16**, all the devices reside in the same package as all the devices are integrated into the same chipset (col. 3, lines 39-55).

Response to Arguments

17. Applicant's arguments filed 11/30/2007 have been fully considered but they are not persuasive.

18. Applicant asserts that Wallace, alone or in combination with Lucas, does not teach an array where at least some of the elements in the array are interconnected so as to make a circuit by determining a state of all of the switches connecting the elements, and where at least some of the elements in the array are formed on a substrate using MEMS technology.

19. However, as explained in the rejection of claims 1 and 2 above, Wallace does teach an array where at least some of the elements in the array are interconnected so as to make a circuit by determining a state of all of the switches connecting the elements. Wallace teaches the use of a filter array (col. 8, lines 13 – col. 10, line 7). The filter is broken into segments separated by transistor switches (T1, T2, T3, etc.; col. 9, lines 3 – 22). The state of these transistors (on or off) determines the final filter circuit

that will alter an input signal of the adjustable multi-stage filter circuit. The transistors each contribute.

20. Further, the limitation wherein "some of said elements are produced on a substrate by utilizing Micro Electro-Mechanical System technology," is considered to be a product-by-process limitation. Even though product-by-process claims are limited by and defined by the process, determination of patentability is based on the product itself. The patentability of a product does not depend on its method of production. If the product in the product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product was made by a different process." In re Thorpe, 777 F.2d 695, 698, 227 USPQ 964, 966 (Fed. Cir. 1985), MPEP 2113.

21. The product structure as claimed is anticipated by the device of Wallace, and further in view of Lucas. Also, the elements (such as a resistor) of Wallace could have been made by a MEMS processes, such as polyMUMPs.

Conclusion

22. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to MICHAEL DURBIN whose telephone number is (571)272-9766. The examiner can normally be reached on M-T 7:30-5; 1st Fri. of biweek off, 2nd 7:30-4.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ken Parker can be reached on (571) 272-2298. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Michael Durbin/
Examiner, Art Unit 2815

/Matthew C. Landau/
Primary Examiner, Art Unit 2815